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(54) Method for recording and playing back a video signal by means of a video cassette recorder and apparatus for carrying out said method.

(57) In the method according to the invention, the recording is performed without any special precautions. An apparatus is connected to the reconstruction output of the video cassette recorder during playback.

It comprises means 30, 36, 40, 45, 70 for storing the video signal VE reconstructed by the video cassette recorder, means 75, 65, 85, 80 for detecting a registration error with regard to video signal VE, and means 50, 55, 70 controlled by said detection means 80 for reconstructing a stored video correction signal VS.

Such a method is used to store infrared signals for various applications, particularly aerospace and medical applications.

The present invention is directed, first, to a method for recording and playing back a video signal to be reconstructed by means of at least one video cassette recorder.

Such a method is useful when it is desired to use a conventional, commercial video cassette recorder (VCR) to record and store and subsequently reconstruct video signals whose characteristics are not those of the television video signals for which the VCR was intended. Such signals are, for example, those delivered by an infrared imaging system for various applications, particularly aerospace and medical applications. These signals, which will be referred to hereinafter as "IR video signals," differ from television video signals, hereinafter referred to as "TV video signals," primarily by their "line" period. For instance, the "line" period of an IR video signal could be 1.5 ms, for example, whereas the "line" period of a TV video signal is 64 μs under the French standard.

A conventional, commercial VCR cannot be used to record and play back an IR video signal without precautions for the following reasons.

In a VCR having at least one head, constraints related to the fact that the running speed of the magnetic tape is limited dictate the use of a complex system for moving the magnetic head relative to the tape. This movement is such that the trace of the head on the tape consists of a succession of tracks inclined relative to the axis of the tape, each track beginning at one edge of the tape and ending at the other edge. Passing from one track to the next, i.e., changing tracks, frequently causes errors that appear when the recorded video signal is played back. This is because variations in the diameter of the drive drums from one VCR to the next or, further, variations in the tension and length of the tape due to differences in temperature and humidity result in poor timing of the beginning of one track relative to the end of the previous one, even in cases where one and the same device is being used for recording and playback. This can occur during recording and during playback. The effect appears during the playback of data recorded near the track change, which are played back too soon or too late, causing the lines to be expanded or compressed in time. An error of this kind will be referred to in the remainder of the text as a "registration error."

Registration errors are not troublesome in connection with the TV video signals for which VCRs are intended, since the period of a track, which is on the order of 20 ms, corresponds to one TV frame. Thus the track change also takes place between two frames, and the registration error that can result affects only lines that are not displayed on the screen.

This is not true of the above-mentioned IR video signal, with which only about thirteen lines per track can be laid down. Thus, without special precautions the IR video signal recorded and then played back on a conventional VCR will have an average of one line out of thirteen that is affected by a registration error. The quality of the reconstructed image will be greatly affected by this.

A method for recording and playing back an IR video signal on a VCR that enables good image quality to be obtained is already known. This method was inspired by that used with a TV video signal. It consists in synchronizing the analysis system delivering the IR video signal and the VCR during recording in such a way that track changes occur during the "idle times" for which the analysis system is not delivering any data for display. The playback is then performed without any special precautions.

This known method has two drawbacks, however. First, it requires the use in the infrared analysis system of motors whose speed can be controlled, i.e., d.c. motors. Such motors are necessarily equipped with brush contacts that are subject to wear and that do not operate satisfactorily at high altitudes, particularly on board the aircraft where the infrared analysis system may be used. Moreover, the idle times are unusable, since there are generally other signals that it would be desirable to be able to record during these idle times.

The present invention is intended to remedy these drawbacks.

To this end, the invention is directed to a method for recording and playing back a video signal to be reconstructed by means of at least one video cassette recorder provided with a magnetic tape, in which the recording is done on a series of magnetic tracks, each track extending from one edge of the tape to the other and each track change potentially generating a registration error, said method being characterized by the fact that the registration errors are detected during playback and corrected before the video signal is reconstructed.

Thus, the recording can be performed without the need to synchronize the infrared analysis system and the VCR.

In addition, the entire length of each track can be used to record useful data.

It is in this aspect that the invention of the present application is remarkable, moreover, since the prior art teaches that the areas adjacent the track changes must be considered improper for recording useful data.

Advantageously, the registration errors affecting the lines are detected by measuring the period of each line and comparing it with a reference period.

In the preferred implementation of the method of the invention, each registration error is corrected by replacing the line affected by it with the previous line.

Thus, given that one line out of thirteen, for example, is affected by a registration error, the line affected by an error is certain to be preceded by a line that has no errors.

The result is a method that is relatively simple to implement and permits the reconstruction of good-quality images.

The present invention also concerns an apparatus for carrying out the method according to the invention for recording and playing back a video signal to be reconstructed by means of at least one video cassette recorder, said apparatus being connected to the reconstruction output of the video cassette recorder, characterized by the fact that it comprises means for storing the video signal reconstructed by the VCR, means for detecting a registration error with regard to said reconstructed and therefore stored video signal, and means, controlled by said detection means, for reconstructing a stored video correction signal.

Advantageously, the means for storing the video signal reconstructed by the VCR comprise two identical memories, each having a capacity corresponding to one line.

Further advantageously, the means for reconstructing a stored video correction signal comprise control circuits for the two memories, adapted so that the same memory is read twice in succession in the event that a registration error is detected.

Still advantageously, the means for detecting a registration error comprise means for measuring the period of each line and means for comparing this period with a reference period.

In the preferred embodiment of the apparatus according to the invention, the means for storing the video signal reconstructed by the VCR comprise an analog-to-digital converter and

two digital memories, and the means for reconstructing the stored video correction signal comprise a digital-to-analog converter.

The invention will be better understood with the aid of the following description of the preferred embodiment of the apparatus of the invention and the method for its use, which description is made with reference to the annexed drawings, wherein:

· Fig. 1 is a block diagram of the apparatus of the invention;

· Fig. 2 is a block diagram of the digital sync word processing circuit of the apparatus of Fig. 2; and

· Fig. 3 is a block diagram of the clock control circuit of the apparatus of Fig. 2.

Referring to Fig. 1, an apparatus for recording and playing back a video signal is connected to the reconstruction output of a VCR, which delivers a signal VE. The reconstruction output of the VCR is connected to the input of an analog-to-digital converter 20 and to the input of a synchronization processing and extraction circuit 10.

The output of the analog-to-digital converter 20 is connected to a bus 21 comprising plural parallel conductors. A first output of line synchronization extraction circuit 10, which delivers a signal S, is connected to a conductor 22. Bus 21 and conductor 22 form a bus 23, connected to the inputs of two buffers 30 and 35. The output of buffer 30 is connected by a bus 31 to the input-output access of a memory 40, here a RAM, and to the input of a buffer 50. The output of buffer 35 is connected by a bus 36 to the input-output access of a memory 45, here a RAM, and to the input of a buffer 55.

Each memory 40 and 45 has a capacity permitting the recording of one line.

The outputs of buffers 50 and 55 are linked by a bus 51 containing a conductor 52 that corresponds to conductor 22, i.e., the one serving as a medium for signal S when buffers 30 and 50, for example, have been successively enabled; conductor 52 is separated from bus 51 and constitutes the sync output S of the apparatus. Bus 51, minus conductor 52, forms bus 53 connected to the input of a digital-to-analog converter 60 whose output delivers the output signal VS of the apparatus.

The first output of line synchronization extraction circuit 10, which delivers signal S, is also connected to the first input of a clock control circuit 70.

Four first outputs of the clock control circuit 70, delivering respectively the signals A, B, C, D, are respectively connected to the first inputs of buffers 30, 35, 50 and 55.

A fifth output of clock control circuit 70, delivering a clock signal H, is connected to the second inputs of buffers 30, 35, 50 and 55, as well as to the count input of a counter 75 and the count-down input of a count-down counter 65.

A sixth output of clock control circuit 70, delivering a sync signal S', is connected to the reset

input of counter 75, to the loading control input of count-down counter 65, to the loading control input of a register 85 and to the first input of a microprogrammed control circuit 80.

A seventh output of clock control circuit 70 is connected by a bus 71 to the clock write inputs and read or write mode command inputs of memories 40 and 45.

The output of counter 75 is connected by a bus 76 to the addressing inputs of memories 40 and 45 and to the loading input of count-down counter 65.

The output of count-down counter 65 is connected by a bus 66 to the input of register 85.

The output of register 85 is connected by a bus 86 to a second input of microprogrammed control circuit 80.

The output of microprogrammed control circuit 80, delivering a signal BB, is connected to a second input of clock control circuit 70.

The second output of synchronization processing and extraction circuit 10, delivering a signal BA, is here connected to a third input of microprogrammed control circuit 80.

Referring now to Fig. 2, the synchronization processing and extraction circuit 10 will now be described.

The input of circuit 10, which receives signal VE, is connected to the input of a transcoding circuit 11 for transcoding a bipolar signal into a binary signal and a clock signal, connected by a binary output V' and a clock output H to a binary input and a clock input, respectively, of a comparison circuit 12.

Comparison circuit 12 comprises, in a known manner, an offset register, here a 16-bit register, and means for comparing the contents of this register with the contents of a programmable memory, said means being connected to a first output of comparison circuit 12 that is connected, via a delay circuit 13 and a monostable circuit 14, to an input of an AND gate 15 whose other input is connected to the binary output V' of transcoding circuit 11. The comparison means are also connected to a second output of comparison circuit 12 that is connected to the second output BA of circuit 10.

AND gate 16 is connected to the input of a counter 16, here a four-digit counter, whose overflow output is connected to output S of circuit 10.

Referring now to Fig. 3, the clock control circuit 70 will now be described.

The first input of circuit 70, that receiving signal S, is connected to the input of a monostable circuit 72 whose output constitutes the sixth output of clock control circuit 70, which delivers signal S'.

The output of a clock 73, whose slave input here is connected to the output of monostable circuit 72, delivers signal H via the fifth output of clock control circuit 70.

The first four outputs and the seventh output of circuit 70 are constituted by the outputs of a combinatorial logic circuit 74 whose three inputs are connected to the output of clock 73, to the output of monostable circuit 72 and to the output of microprogrammed control circuit 80.

Microprogrammed control circuit 80 is a microprocessor here.

The apparatus that has just been described, for implementing the method according to the invention for recording and playing back a video signal by means of at least one VCR, operates in the following manner.

The apparatus is not used during the recording of the video signal, which is performed in the conventional manner and without special precautions, and particularly without synchronization between the VCR and the analysis system delivering the video signal.

During playback, the apparatus just described is interposed between the reconstruction output of the VCR and the input of the user device, for example a cathode-ray-tube display system or a system for reconstructing the data on film.

Since the recording was done without special precautions, some lines of signal VE reconstructed by the VCR are affected by registration errors. The apparatus just described, to which signal VE is applied, detects each of these lines and replaces it with the previous line, thus delivering a VS signal in which no line is affected by a registration error.

This result is obtained in the following manner.

The analog video signal VE is converted into a digital video signal by analog-to-digital converter 20. Both this digital video signal and the line sync output signal S of synchronization processing and extraction circuit 10 are sent via bus 23 to the inputs of buffers 30 and 35.

For the present, and to facilitate comprehension, we will assume that the lines making up signal VE have no registration errors, and we will consider the instant at which the digital video signal begins to describe the line of row n - 1, the instant defined by the sync pulse corresponding to signal S.

Clock control circuit 70 then commands:

- buffer 30 to go to the enabled state, by means of signal A;
- buffer 35 to go to the disabled state, by means of signal B;
- memory 40 to go into write and clock write mode, via bus 71;
- buffer 50 to go to the disabled state, by means of signal C.

The line of row n - 1 thus is entered in memory 40 at the addresses generated by counter 75, which counts the clock pulses in signal H, starting from the reset corresponding to the sync bit of signal S', which occurs at the same time as the sync pulse of signal S.

When the sync pulse corresponding to the beginning of the line of row n occurs, clock control

circuit 70 then commands:

- buffer 30 to go to the disabled state, by means of signal A;
- buffer 35 to go to the enabled state, by means of signal B;
- memory 40 to go into read mode, via bus 71;
- memory 45 to go into write and clock write mode, via bus 71;
- buffer 50 to go to the enabled state, by means of signal C;
- buffer 55 to go to the disabled state, by means of signal D.

Thus, while the line of row n is being entered in memory 45, addressed by counter 75 as in the case of memory 45, the contents of memory 40, constituted by the line of row n - 1, are read and transferred via buffer 50 and buses 51 and 53 to digital-to-analog converter 60, which converts them into an analog signal VS.

When the sync pulse corresponding to the beginning of the line of row n + 1 occurs an identical sequence takes place, but with the roles of buffers 30 and 35, memories 40 and 45 and buffers 50 and 55 reversed. The line of row n + 1 is entered in memory 40 while the contents of memory 45, constituted by the line of row n, are transferred as output to the input of digital-to-analog converter 60.

Thus, in the absence of any registration errors, analog signal VS duplicates analog signal VE with a time lag equal to the period of one line.

Any registration errors are detected by means of count-down counter 65, register 85 and microprogrammed control circuit 80. When the sync bit of signal S' corresponding to the beginning of the line of row n occurs, counter 75 has counted a number L_{n-1} of clock pulses in signal H which corresponds to the period of the line of row n - 1, and this number is loaded into count-down counter 65. At the end of the line of row n, the output of counter 75 is L_n, corresponding to the period of the line of row n, and the output of the count-down counter is equal to the difference:

$$\Delta_n = L_n - L_{n-1}$$

When the sync bit of signal S' corresponding to the beginning of the line of row n + 1 occurs, the number Δ_n is loaded into register 85. Microprogrammed control circuit 80 compares the absolute value of this number $|\Delta_n|$ to a suitably selected threshold Δ_{no}. This is obtained by determining the threshold Δ_{no} for which the case

$$|\Delta_n| \leq \Delta_{no}$$

corresponds to the absence of registration errors or to an imperceptible registration error, and the case

$$|\Delta_n| > \Delta_{no}$$

corresponds to a troublesome error.

Thus, the period of the line of row n is compared with a reference period, which in this case is the period of the line of row n - 1.

If the first case ($|\Delta_n| > \Delta_{no}$) is present, signal BB from microprogrammed control circuit 80 remains at the zero level and the manner of operation of clock control circuit 70 is as described above.

If, on the other hand, Δ_n corresponds to a registration error, microprogrammed control circuit 80 emits a signal BB at level "one" -- "a disabling bit" -- which modifies the operation of clock control circuit 70 such that, contrary to what took place in the preceding case, the states of buffers 30, 35, 50 and 55 and the modes of memories 40 and 45 remain the same during the arrival of line n + 1 as they were during the arrival of line n, i.e.:

· buffer 30 in the disabled state;

· buffer 35 in the enabled state;

· memory 40 in read mode;

· memory 45 in write mode;

· buffer 50 in the enabled state;

· buffer 55 in the disabled state.

Thus, the line of row n + 1 is entered in memory 45 in place of the line of row n, while the contents of memory 40, constituted by the line of row n - 1, are read and transferred as output. In signal VS, the line of row n is replaced by the line of row n - 1, which is free of registration errors, since the line of row n is affected by a registration error and it is impossible for two consecutive lines to be disrupted.

It will be noted that, given the method used to detect a registration error, when the line of row n is affected by an error, the microprogrammed control circuit does in fact detect

$$|\Delta_n| > \Delta_{no},$$

but it also detects, in the next line:

$$|\Delta_n + 1| > \Delta_{no}$$

since

$$\Delta_{n+1} = L_{n+1} - L_n,$$

L_{n+1} necessarily being correct and L_n incorrect.

The microprogrammed control circuit is therefore adapted not to generate two disabling bits corresponding to two successive lines, so that the line of row n + 1, which is correct, is not replaced by the line of row n, which is affected by an error.

The apparatus currently being described further includes an advantageous but not indispensable characteristic which makes it feasible in certain specific cases to reduce the percentage of lines rejected and thus to further improve the quality of the image.

These specific cases are situations in which the end of each line of the video signal to be processed is a digital sync word, which is not a part that is to be displayed. Since this word is the same at the end of each line, it is of no great consequence if it is affected by a registration error. Moreover, when this word is affected by a registration error, the part of the line that is to be displayed is certain not to affected, despite the positive detection made by microprogrammed

control circuit 80.

Thus, synchronization processing and extraction circuit 10 is adapted to detect a registration error that occurs during the digital sync word. If this is the case, signal BA passes to level one. Microprogrammed control circuit 80 interprets this signal by canceling the disabling bit being sent to clock control circuit 70. Hence, the line during which the error occurred during the digital sync word will not be rejected.

The synchronization processing and extraction circuit 10 operates as follows. The digital sync word located at the end of each line, encoded bipolarly in this case, is converted by transcoder 11 into a binary word, which, after being input serially into the offset register of comparison circuit 12, is identified, here to within two bits, by this comparison circuit 12, which delivers a pulse via its first output. This pulse is delayed by a time τ by delay circuit 13. Time τ corresponds to the time interval normally separating the digital sync word at the end of one line from the beginning of a train of, here, four sync pulses starting the next line. The monostable circuit normally allows the four sync pulses to pass through AND gate 15; they are counted by counter 16, which then delivers the line sync pulse, i.e., signal S, via the first output of synchronization processing and extraction circuit 10.

In addition, the comparison circuit is adapted to deliver a pulse via the second output BA of synchronization processing and extraction circuit 10 when the digital sync word is not rigorously exact.

Furthermore, clock control circuit 70, which comprises a clock 73 here slaved to the line frequency, could instead comprise an unslaved clock.

Likewise, memories 40 and 45, which are RAMs here, could be replaced by any other type of memory.

Moreover, sync signal S is here available in separate form as output from the apparatus via conductor 52, since this signal is generally necessary for the display systems used, but the output of the apparatus could be constituted solely by signal VS.

Also, if the video signal is available in digital form at the input of the apparatus, or conversely if it is desired for the apparatus to output a digital video signal, it is, of course, feasible to provide input and output points downstream from analog-to-digital converter 20 or upstream from digital-to-analog converter 60.

Finally, in the foregoing description it has been assumed that the same VCR was used for recording and playback; this is not necessary for implementing the method of the invention, and first VCR can be used for recording while a second VCR is used for playback, for example.

CLAIMS

1. A method for recording and playing back a video signal to be reconstructed by means of at least one video cassette recorder provided with a magnetic tape, wherein the recording is done on a series of magnetic tracks, each track extending from one edge of the tape to the other and each track change potentially generating a registration error, said method being characterized by the fact that the registration errors are detected during playback and corrected before the video signal is reconstructed.

2. The method as recited in claim 1, wherein the registration errors affecting the lines are detected by measuring the period of each line and comparing it with a reference period.

3. The method as recited in claim 3, wherein said reference period is the period of the previous line.

4. The method as recited in one of claims 1 to 3, wherein each registration error is corrected by replacing the line that it affects with the previous line.

5. The method as recited in one of claims 1 to 4, wherein the reconstruction of the video signal is offset in time by the period of one line, relative to playback.

6. An apparatus for carrying out the method according to claim 1 for recording and playing back a video signal to be reconstructed by means of at least one video cassette recorder provided with a magnetic tape, said apparatus being connected to the reconstruction output of said video cassette recorder, characterized by the fact that it comprises means (30, 35, 40, 45, 70) for storing the video signal (VE) reconstructed by said video cassette recorder, means (75, 65, 85, 80) for detecting a registration error in said reconstructed and therefore stored video signal (VE), and means (50, 55, 70), controlled by said detection means (80), for reconstructing a stored video correction signal (VS).

7. The apparatus as recited in claim 6, wherein said means for storing said video signal (VE) reconstructed by said video cassette recorder comprise two identical memories (40, 45), each having a capacity permitting the recording of one line.

8. The apparatus as recited in claim 7, wherein said means for reconstructing a stored video correction signal (VS) comprise control circuits (50, 55, 70, 80) of said memories (40, 45), adapted so that the same memory is read twice in succession in the event that a registration error is detected.

9. The apparatus as recited in one of claims 6 to 8, wherein said means (75, 65, 85, 80) for detecting a registration error comprise a microprogrammed control circuit (80) adapted so that after an error as been detected in one line it disables detection in the next line.

10. The apparatus as recited in one of claims 6 to 9, wherein the means for detecting a registration error comprise means (75) for measuring the period of each line and means (65, 85, 80) for comparing said period with a reference period.

11. The apparatus as recited in one of claims 6 to 10, wherein said means for storing said video signal (VE) reconstructed by said video cassette recorder comprise an analog-to-digital converter (20) and at least one digital memory (40, 45) and said means for reconstructing said stored video correction signal comprise a digital-to-analog converter (60).